

CLAIMS:

1. Memory integrated circuitry comprising:

an array of memory cells formed in lines over a semiconductive substrate and occupying area thereover, the respective area consumed by at least some individual memory cells within the array being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

2. The memory integrated circuitry of claim 1 wherein the memory cells comprise DRAM cells.

3. The memory integrated circuitry of claim 1 wherein individual of the lines of memory cells are substantially straight throughout the array.

1 4. The memory integrated circuitry of claim 1 wherein the
2 LOCOS field oxide between adjacent lines is less than or equal to 2500
3 Angstroms thick.

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5 5. The memory integrated circuitry of claim 1 wherein said
6 respective area consumed by at least some individual memory cells
7 within the array is no greater than about $7F^2$.

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9 6. The memory integrated circuitry of claim 1 wherein said
10 respective area consumed by at least some individual memory cells
11 within the array is no greater than about $6F^2$.

1 7. Memory integrated circuitry comprising:

2 an array of memory cells formed over a semiconductive substrate
3 and occupying area thereover, at least some memory cells of the array
4 being formed in lines of active area formed within the semiconductive
5 substrate which are continuous between adjacent memory cells, said
6 adjacent memory cells being isolated from one another relative to the
7 continuous active area formed therebetween by a conductive line formed
8 over said continuous active area between said adjacent memory cells;

9 the respective area consumed by individual of said adjacent
10 memory cells being equal to less than $8F^2$, where "F" is no greater
11 than 0.25 micron and is defined as equal to one-half of minimum pitch,
12 with minimum pitch being defined as equal to the smallest distance of
13 a line width plus width of a space immediately adjacent said line on
14 one side of said line between said line and a next adjacent line in a
15 repeated pattern within the array; and

16 at least some of the minimum pitch adjacent lines of memory
17 cells within the array being isolated from one another by LOCOS field
18 oxide formed therebetween.

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20 8. The memory integrated circuitry of claim 7 wherein
21 individual of the lines of continuous active area are substantially straight
22 throughout the array.

1 9. The memory integrated circuitry of claim 7 wherein the
2 LOCOS field oxide between adjacent lines is less than or equal to 2500
3 Angstroms thick.

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5 10. The memory integrated circuitry of claim 7 wherein the
6 memory cells comprise DRAM cells.

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8 11. The memory integrated circuitry of claim 7 wherein said
9 respective area consumed by at least some individual memory cells
10 within the array is no greater than about $7F^2$.

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12 12. The memory integrated circuitry of claim 7 wherein said
13 respective area consumed by at least some individual memory cells
14 within the array is no greater than about $6F^2$.

1 13. Dynamic random access memory circuitry comprising:
2 an array of word lines and bit lines formed over a semiconductive
3 substrate defining an array of DRAM cells occupying area over the
4 semiconductive substrate, at least some DRAM cells of the array being
5 formed in lines of active area formed within the semiconductive
6 substrate beneath the word lines and which are continuous between
7 adjacent DRAM cells, said adjacent DRAM cells being isolated from
8 one another relative to the continuous active area formed therebetween
9 by a conductive line formed over said continuous active area between
10 said adjacent DRAM cells;

11 the respective area consumed by individual of said adjacent
12 memory cells being equal to less than $8F^2$, where "F" is no greater
13 than 0.25 micron and is defined as equal to one-half of minimum pitch,
14 with minimum pitch being defined as equal to the smallest distance of
15 a line width plus width of a space immediately adjacent said line on
16 one side of said line between said line and a next adjacent line in a
17 repeated pattern within the array; and

18 at least some of the minimum pitch adjacent lines of memory
19 cells within the array being isolated from one another by LOCOS field
20 oxide formed therebetween; and

21 the bit lines comprise D and D* lines formed in a folded bit line
22 architecture within the array.
23
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1 14. The memory integrated circuitry of claim 13 wherein
2 individual of the lines of continuous active area are substantially straight
3 throughout the array.

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5 15. The memory integrated circuitry of claim 13 wherein the
6 LOCOS field oxide between adjacent lines is less than or equal to 2500
7 Angstroms thick.

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9 16. The memory integrated circuitry of claim 13 wherein said
10 respective area consumed by at least some individual memory cells
11 within the array is no greater than about $7F^2$.

12
13 17. The memory integrated circuitry of claim 13 wherein said
14 respective area consumed by at least some individual memory cells
15 within the array is no greater than about $6F^2$.

1 18. Dynamic random access memory circuitry comprising:

2 an array of word lines and bit lines formed over a bulk silicon
3 semiconductive substrate defining an array of DRAM cells occupying
4 area over the semiconductive substrate, the word lines and bit lines
5 having respective conductive widths which are less than or equal to 0.25
6 micron, the DRAM cells within the array being formed in lines of
7 active area formed within the silicon substrate beneath the word lines
8 and which are continuous between adjacent DRAM cells, said adjacent
9 DRAM cells being isolated from one another relative to the continuous
10 active area formed therebetween by respective conductive lines formed
11 over said continuous active area between said adjacent DRAM cells;

12 at least some adjacent lines of continuous active area within the
13 array being isolated from one another by LOCOS field oxide formed
14 therebetween, said LOCOS field oxide having a thickness of no greater
15 than 2500 Angstroms;

16 the respective area consumed by individual of said adjacent
17 memory cells being equal to less than 0.5 micron²; and

18 the bit lines comprise D and D* lines formed in a folded bit line
19 architecture within the array.
20

21 19. The memory integrated circuitry of claim 18 wherein
22 individual of the lines of continuous active area are substantially straight
23 throughout the array.
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1 20. The memory integrated circuitry of claim 18 wherein said
2 respective area consumed by at least some individual memory cells
3 within the array is no greater than 0.4375 micron².

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5 21. The memory integrated circuitry of claim 18 wherein said
6 respective area consumed by at least some individual memory cells
7 within the array is no greater than 0.375 micron².

1 22. Dynamic random access memory circuitry comprising:

2 an array of word lines and bit lines formed over a semiconductive
3 substrate defining an array of DRAM cells occupying area over the
4 semiconductive substrate, at least some DRAM cells of the array being
5 formed in lines of active area formed within the semiconductive
6 substrate beneath the word lines and which are continuous between
7 adjacent DRAM cells, said adjacent DRAM cells being isolated from
8 one another relative to the continuous active area formed therebetween
9 by a conductive line formed over said continuous active area between
10 said adjacent DRAM cells;

11 the respective area consumed by individual of said adjacent
12 memory cells being equal to less than $8F^2$, where "F" is defined as
13 equal to one-half of minimum pitch, with minimum pitch being defined
14 as equal to the smallest distance of a line width plus width of a space
15 immediately adjacent said line on one side of said line between said
16 line and a next adjacent line in a repeated pattern within the array;
17 and

18 the bit lines comprise D and D* lines formed in a folded bit
19 line architecture within the array.

20
21 23. The memory integrated circuitry of claim 22 wherein
22 individual of the lines of continuous active area are substantially straight
23 throughout the array.

1 24. The memory integrated circuitry of claim 22 wherein F is
2 no greater than 0.25 micron.

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4 25. The memory integrated circuitry of claim 22 wherein said
5 respective area consumed by at least some individual memory cells
6 within the array is no greater than about $7F^2$.

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8 26. The memory integrated circuitry of claim 22 wherein said
9 respective area consumed by at least some individual memory cells
10 within the array is no greater than about $6F^2$.